Computer Organization and Architecture

Referred Book

Computer_ Organization _ and_ Architecture - William Stallings

C h a p t e r **2 COMPUTER EVOLUTION AND PERFORMANCE**

- **Internal structure of IAS Computer or Internal structure of von Neumann's Machine**

Figure shows the general structure of the IAS computer. It consists of

• A main memory, which stores both data and instructions1

• An arithmetic and logic unit (ALU) capable of operating on binary data

• A control unit, which interprets the instructions in memory and causes them to be executed

• Input and output (I/O) equipment operated by the control unit

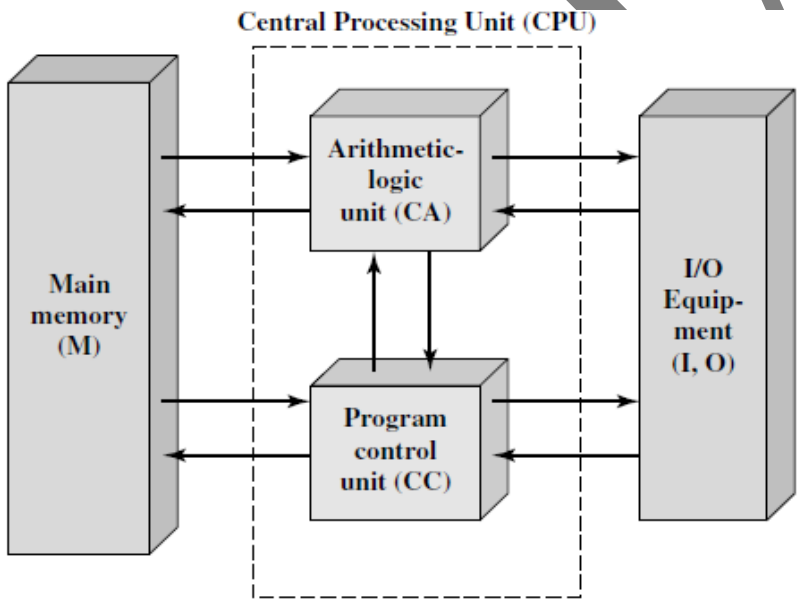

Figure 2.1 Structure of the IAS Computer

- **IAS Memory Format**

The memory of the IAS consists of 1000 storage locations, called *words*, of40 binary digits (bits) each. Both data and instructions are stored there. Numbers are represented in binary form, and each instruction is a binary code. Figure 2.2 illustrates these formats. Each number is represented by a sign bit and a 39-bit value.

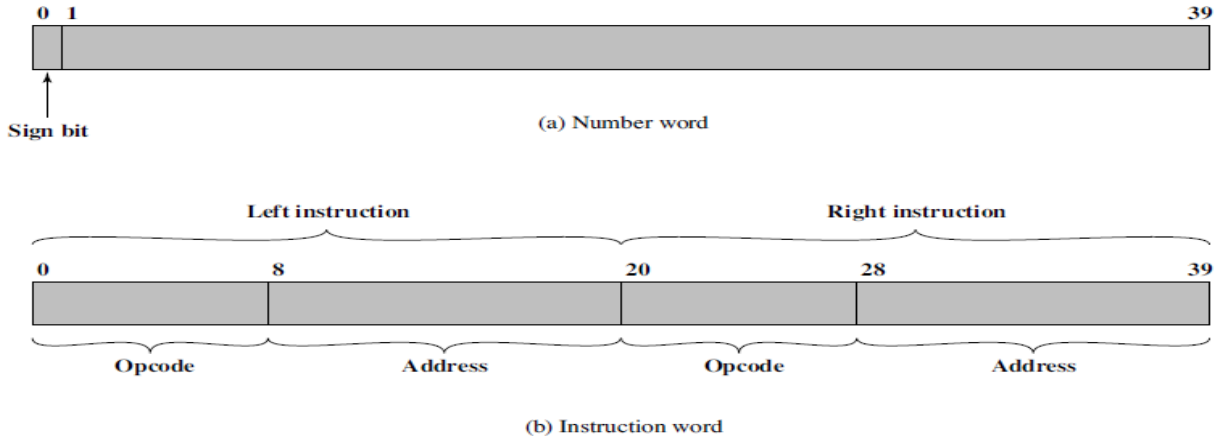

Figure 2.2 IAS Memory Formats

A word may also contain two 20-bit instructions, with each instruction consisting of an 8-bit operation code (op-code) specifying the operation to be performed and a 12-bit address designating one of the words in memory (numbered from 0 to 999).

The control unit operates the IAS by fetching instructions from memory and executing them one at a time.

- **The expanded structure of ISA computer**

Figure 2.3.This figure reveals that both the control unit and the ALU contain storage locations, called *registers,* defined as follows:

• **Memory buffer register (MBR):** Contains a word to be stored in memory or sent to the I/O unit, or is used to receive a word from memory or from the I/O unit.

• **Memory address registers (MAR):** Specifies the address in memory of the word to be written from or read into the MBR.

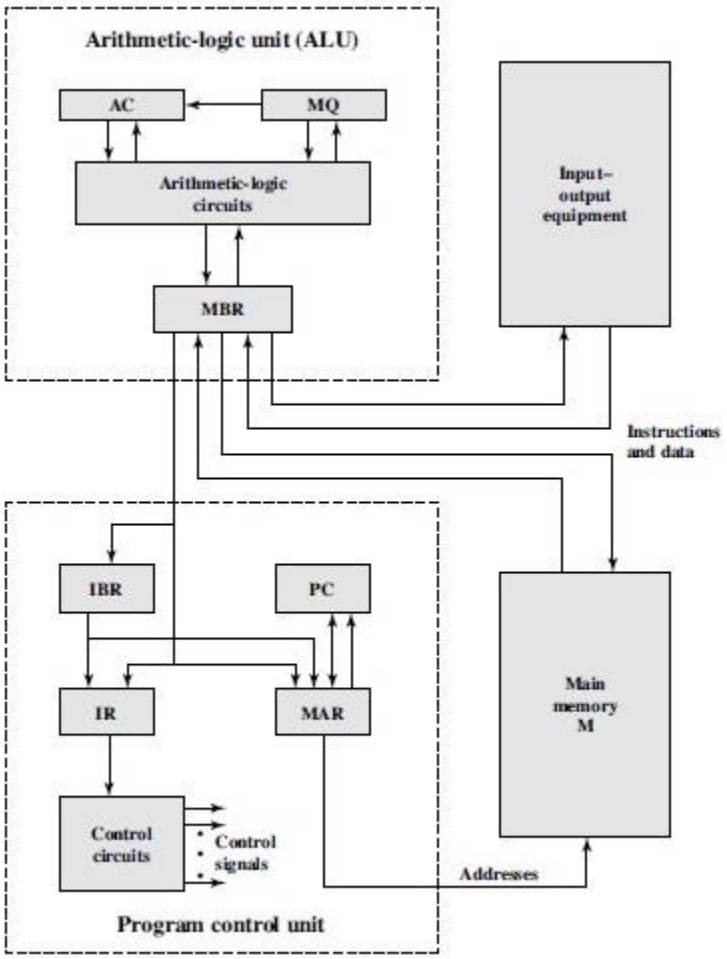

Figure 2.3 Expanded Structure of IAS Computer

• **Instruction register (IR):** Contains the 8-bit op-code instruction being executed.
• **Instruction buffer register (IBR):** Employed to hold temporarily the right hand instruction from a word in memory.
• **Program counter (PC):** Contains the address of the next instruction-pair to be fetched from memory.
• **Accumulator (AC) and multiplier quotient (MQ):** Employed to hold temporarily operands and results of ALU operations. For example, the result of multiplying two 40-bit numbers is an 80-bit number; the most significant 40 bits are stored in the AC and the least significant in the MQ.