C h a p t e r **15 CONTROL UNIT OPERATION**

Micro operation in executing a program consists of a sequence of instruction cycles, with one machine instruction per cycle.

We have further seen that each instruction cycle is made up of a number of smaller units. One subdivision that we found convenient is fetch, indirect, execute, and interrupt, with only fetch and execute cycles always occurring. we will see that each of the smaller cycles involves

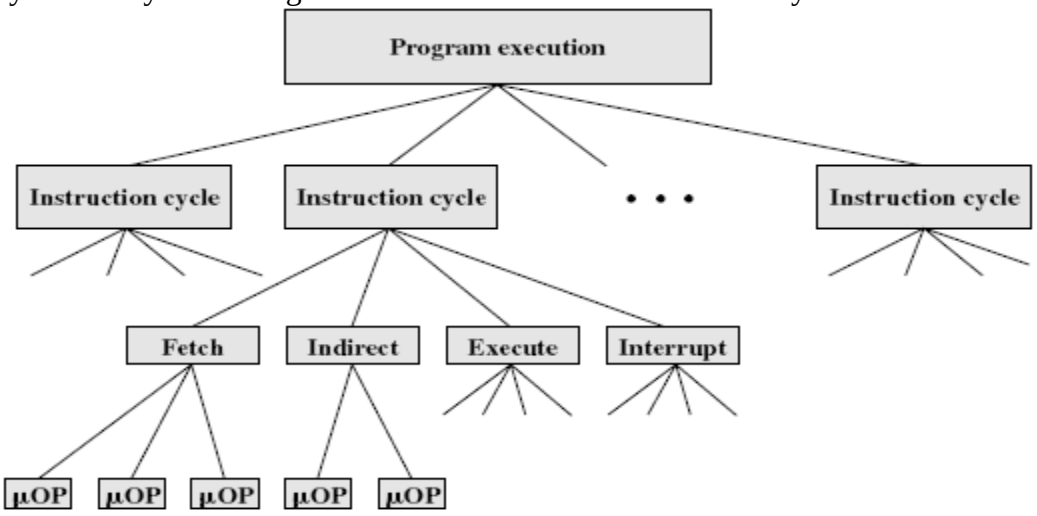

Figure 15.1 Constituent Elements of a Program Execution

To summarize, the execution of a program consists of the sequential execution of instructions. Each instruction is executed during an instruction cycle made up of shorter sub cycles (e.g., fetch, indirect, execute, interrupt).The execution of each sub cycle involves one or more shorter operations, that is, micro-operations.

- **Control Unit**

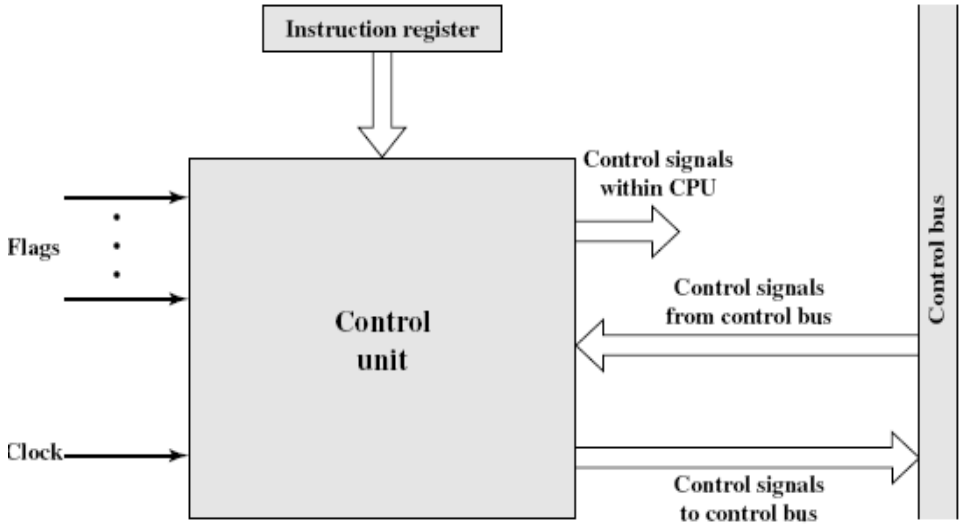

Figure 15.4 Block Diagram of the Control Unit

Figure 15.4 is a general model of the control unit, showing all of its inputs and outputs. The inputs are

• **Clock:** This is how the control unit "keeps time." The control unit causes one micro-operation (or a set of simultaneous micro-operations) to be performed for each clock pulse. This is sometimes referred to as the processor cycle time, or the clock cycle time.

• **Instruction register:** The op-code and addressing mode of the current instruction are used to determine which micro-operations to perform during the execute cycle.

• **Flags:** These are needed by the control unit to determine the status of the processor and the outcome of previous ALU operations. For example, for the increment-and-skip-if-zero (ISZ) instruction, the control unit will increment the PC if the zero flag is set.

• **Control signals from control bus:** The control bus portion of the system bus provides signals to the control unit.

- **Internal Processor Organization**

Using an internal processor bus, Figure 15.5 can be rearranged as shown in Figure 15.6. A single internal bus connects the ALU and all processor registers.

Gates and control signals are provided for movement of data onto and off the bus from each register. Additional control signals control data transfer to and from the system (external) bus and the operation of the ALU.

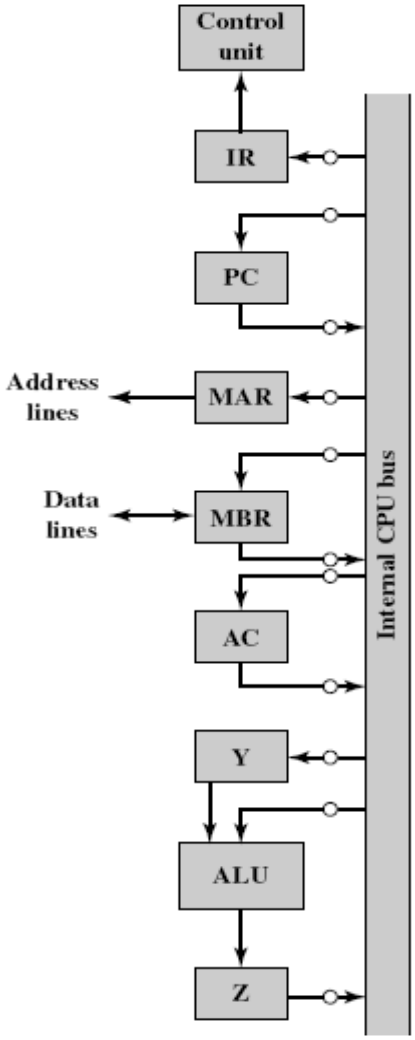

Figure 15.6 CPU with Internal Bus

Two new registers, labeled Y and Z, have been added to the organization. These are needed for the proper operation of the ALU. When an operation involving two operands is performed, one can be obtained from the internal bus, but the other must be obtained from another source. The AC could be used for this purpose,